



# MS-7508Ver:10

## CPU:

AMD AM2 and AM2R2

## System Chipset:

NVIDIA MCP78U/S

## On Board Chipset:

Winbond Super I/O -- FINTEK71882

LAN -- RTL8211BL

HD Codec --ALC888

JIMCRO 1394

BIOS -- SPI ROM

## Main Memory:

DDR 2\*4(Max4GB)

## Expansion Slots:

PCI 2.3 Slot \*2

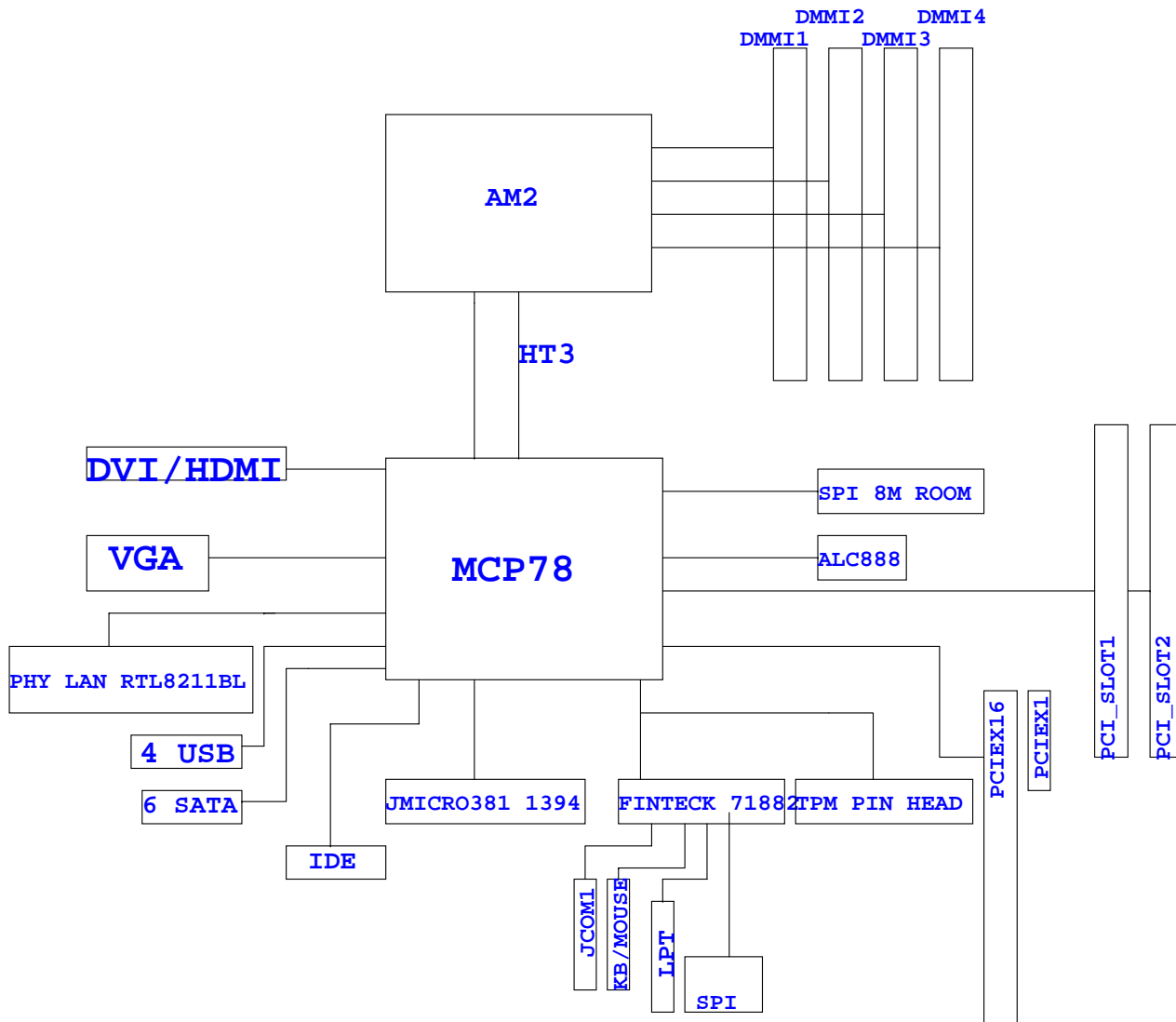
## PWM:

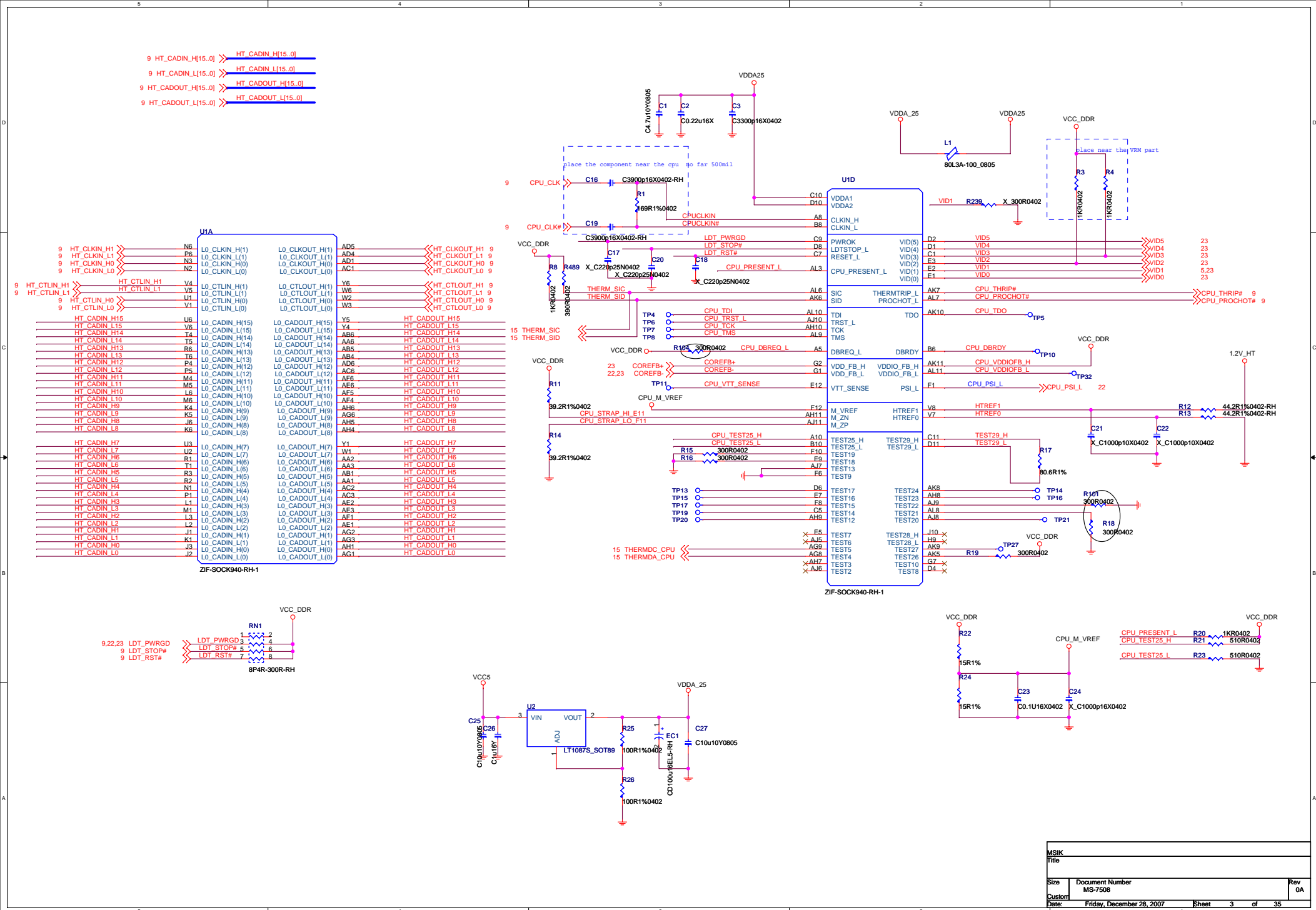
ST6740+ST6741

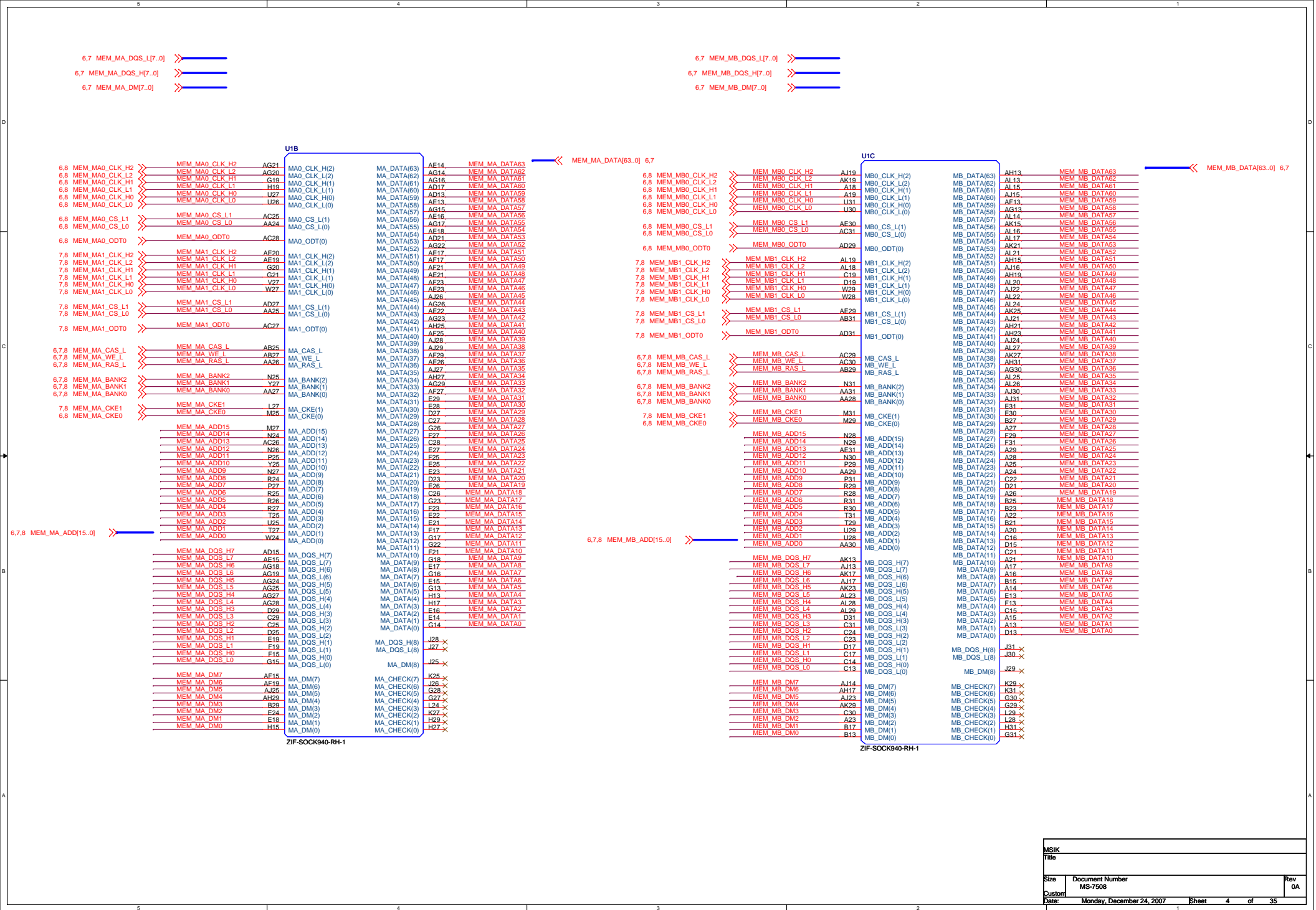
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## NOTE:

all the 0ohm resistor default not stuff ,change footprint as R0402\_6 or R0603\_10 ,for costdown request



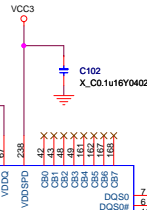






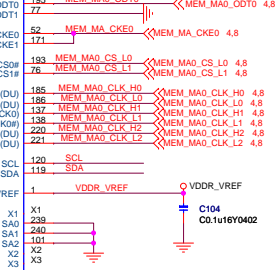
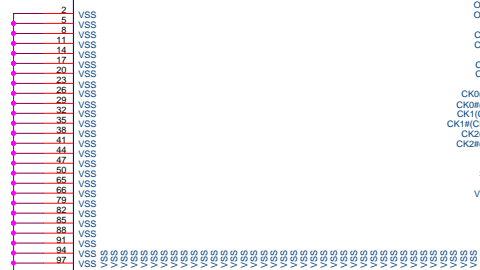
4.7 MEM\_MA\_DQS\_H[7..0] >>  
4.7 MEM\_MA\_DQS\_L[7..0] >>  
4.7 MEM\_MA\_DM[7..0] >>

VCC\_DDR  
C102  
X\_C0.1u16Y0402



MEM_MA_DATA0	3	D00	MEM_MA_DATA0	3	D00
MEM_MA_DATA1	4	D01	MEM_MA_DATA1	4	D01
MEM_MA_DATA2	5	D02	MEM_MA_DATA2	5	D02
MEM_MA_DATA3	6	D03	MEM_MA_DATA3	6	D03
MEM_MA_DATA4	7	D04	MEM_MA_DATA4	7	D04
MEM_MA_DATA5	8	D05	MEM_MA_DATA5	8	D05
MEM_MA_DATA6	9	D06	MEM_MA_DATA6	9	D06
MEM_MA_DATA7	10	D07	MEM_MA_DATA7	10	D07
MEM_MA_DATA8	11	D08	MEM_MA_DATA8	11	D08
MEM_MA_DATA9	12	D09	MEM_MA_DATA9	12	D09
MEM_MA_DATA10	13	D10	MEM_MA_DATA10	13	D10
MEM_MA_DATA11	14	D11	MEM_MA_DATA11	14	D11
MEM_MA_DATA12	15	D12	MEM_MA_DATA12	15	D12
MEM_MA_DATA13	16	D13	MEM_MA_DATA13	16	D13
MEM_MA_DATA14	17	D14	MEM_MA_DATA14	17	D14
MEM_MA_DATA15	18	D15	MEM_MA_DATA15	18	D15
MEM_MA_DATA16	19	D16	MEM_MA_DATA16	19	D16
MEM_MA_DATA17	20	D17	MEM_MA_DATA17	20	D17
MEM_MA_DATA18	21	D18	MEM_MA_DATA18	21	D18
MEM_MA_DATA19	22	D19	MEM_MA_DATA19	22	D19
MEM_MA_DATA20	23	D20	MEM_MA_DATA20	23	D20
MEM_MA_DATA21	24	D21	MEM_MA_DATA21	24	D21
MEM_MA_DATA22	25	D22	MEM_MA_DATA22	25	D22
MEM_MA_DATA23	26	D23	MEM_MA_DATA23	26	D23
MEM_MA_DATA24	27	D24	MEM_MA_DATA24	27	D24
MEM_MA_DATA25	28	D25	MEM_MA_DATA25	28	D25
MEM_MA_DATA26	29	D26	MEM_MA_DATA26	29	D26
MEM_MA_DATA27	30	D27	MEM_MA_DATA27	30	D27
MEM_MA_DATA28	31	D28	MEM_MA_DATA28	31	D28
MEM_MA_DATA29	32	D29	MEM_MA_DATA29	32	D29
MEM_MA_DATA30	33	D30	MEM_MA_DATA30	33	D30
MEM_MA_DATA31	34	D31	MEM_MA_DATA31	34	D31
MEM_MA_DATA32	35	D32	MEM_MA_DATA32	35	D32
MEM_MA_DATA33	36	D33	MEM_MA_DATA33	36	D33
MEM_MA_DATA34	37	D34	MEM_MA_DATA34	37	D34
MEM_MA_DATA35	38	D35	MEM_MA_DATA35	38	D35
MEM_MA_DATA36	39	D36	MEM_MA_DATA36	39	D36
MEM_MA_DATA37	40	D37	MEM_MA_DATA37	40	D37
MEM_MA_DATA38	41	D38	MEM_MA_DATA38	41	D38
MEM_MA_DATA39	42	D39	MEM_MA_DATA39	42	D39
MEM_MA_DATA40	43	D40	MEM_MA_DATA40	43	D40
MEM_MA_DATA41	44	D41	MEM_MA_DATA41	44	D41
MEM_MA_DATA42	45	D42	MEM_MA_DATA42	45	D42
MEM_MA_DATA43	46	D43	MEM_MA_DATA43	46	D43
MEM_MA_DATA44	47	D44	MEM_MA_DATA44	47	D44
MEM_MA_DATA45	48	D45	MEM_MA_DATA45	48	D45
MEM_MA_DATA46	49	D46	MEM_MA_DATA46	49	D46
MEM_MA_DATA47	50	D47	MEM_MA_DATA47	50	D47
MEM_MA_DATA48	51	D48	MEM_MA_DATA48	51	D48
MEM_MA_DATA49	52	D49	MEM_MA_DATA49	52	D49
MEM_MA_DATA50	53	D50	MEM_MA_DATA50	53	D50
MEM_MA_DATA51	54	D51	MEM_MA_DATA51	54	D51
MEM_MA_DATA52	55	D52	MEM_MA_DATA52	55	D52
MEM_MA_DATA53	56	D53	MEM_MA_DATA53	56	D53
MEM_MA_DATA54	57	D54	MEM_MA_DATA54	57	D54
MEM_MA_DATA55	58	D55	MEM_MA_DATA55	58	D55
MEM_MA_DATA56	59	D56	MEM_MA_DATA56	59	D56
MEM_MA_DATA57	60	D57	MEM_MA_DATA57	60	D57
MEM_MA_DATA58	61	D58	MEM_MA_DATA58	61	D58
MEM_MA_DATA59	62	D59	MEM_MA_DATA59	62	D59
MEM_MA_DATA60	63	D60	MEM_MA_DATA60	63	D60
MEM_MA_DATA61	64	D61	MEM_MA_DATA61	64	D61
MEM_MA_DATA62	65	D62	MEM_MA_DATA62	65	D62
MEM_MA_DATA63	66	D63	MEM_MA_DATA63	66	D63

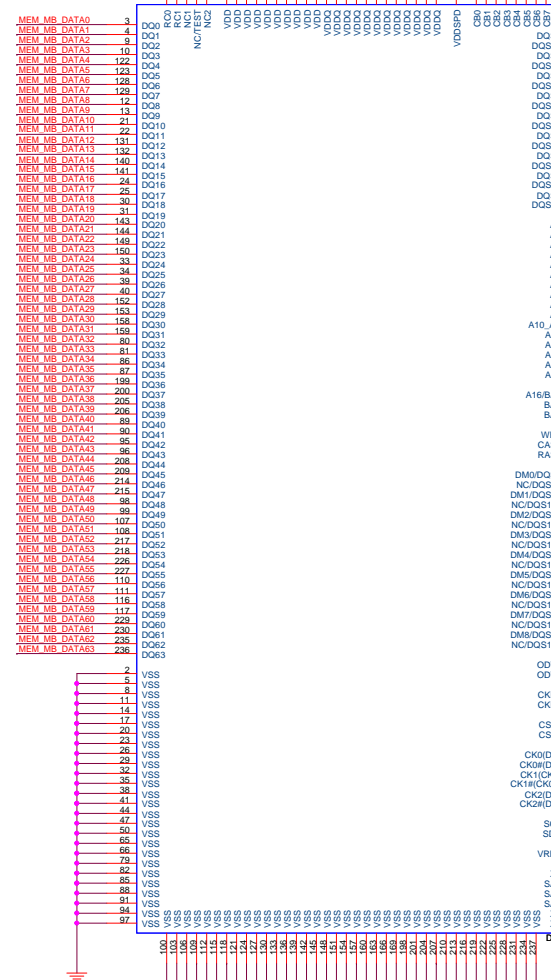
ADDRESS A0



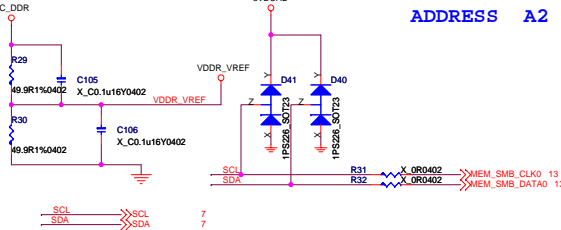
DDR1-240\_0RANG-RH

4.7 MEM\_MB\_DQS\_H[7..0] >>  
4.7 MEM\_MB\_DQS\_L[7..0] >>  
MEM\_MB\_DM[7..0] 4.7  
MEM\_MB\_DATA[63..0] 4.7  
MEM\_MB\_ADD[15..0] 4.7.8

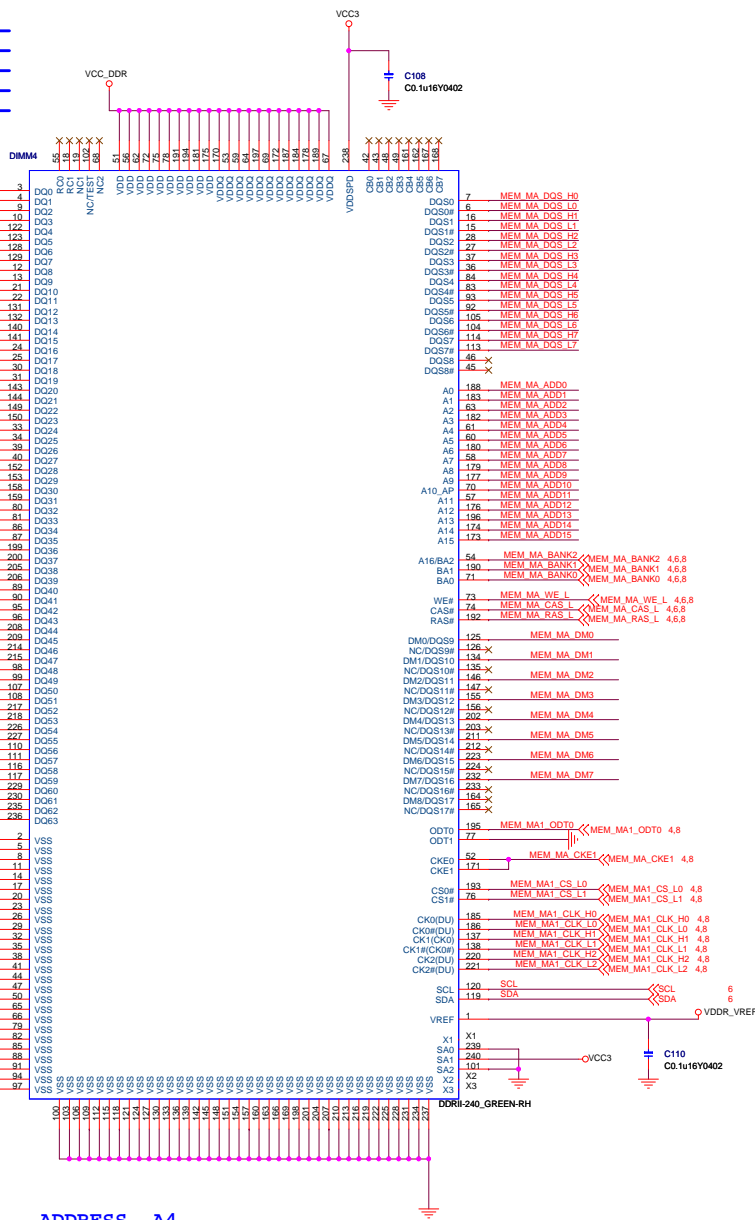
DMM1



ADDRESS A2



4.6 MEM\_MA\_DM[7..0]  
4.6.8 MEM\_MA\_ADD[15..0]  
4.6 MEM\_MA\_DQS\_H[7..0]  
4.6 MEM\_MA\_DQS\_L[7..0]  
4.6 MEM\_MA\_DATA[63..0]



ADDRESS A4

4.6 MEM\_MB\_DM[7..0]  
4.6.8 MEM\_MB\_ADD[16..0]  
4.6 MEM\_MB\_DATA[63..0]

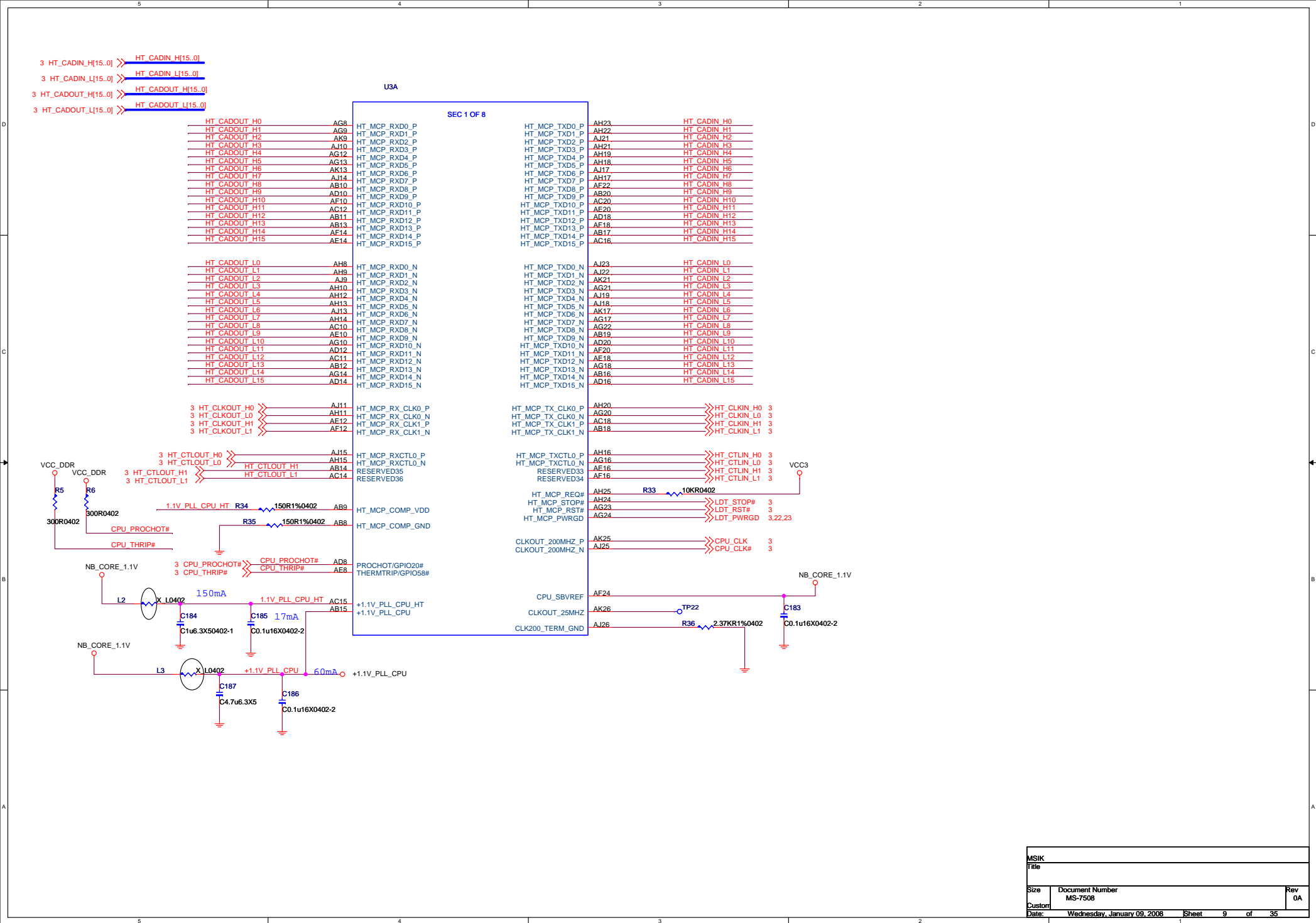


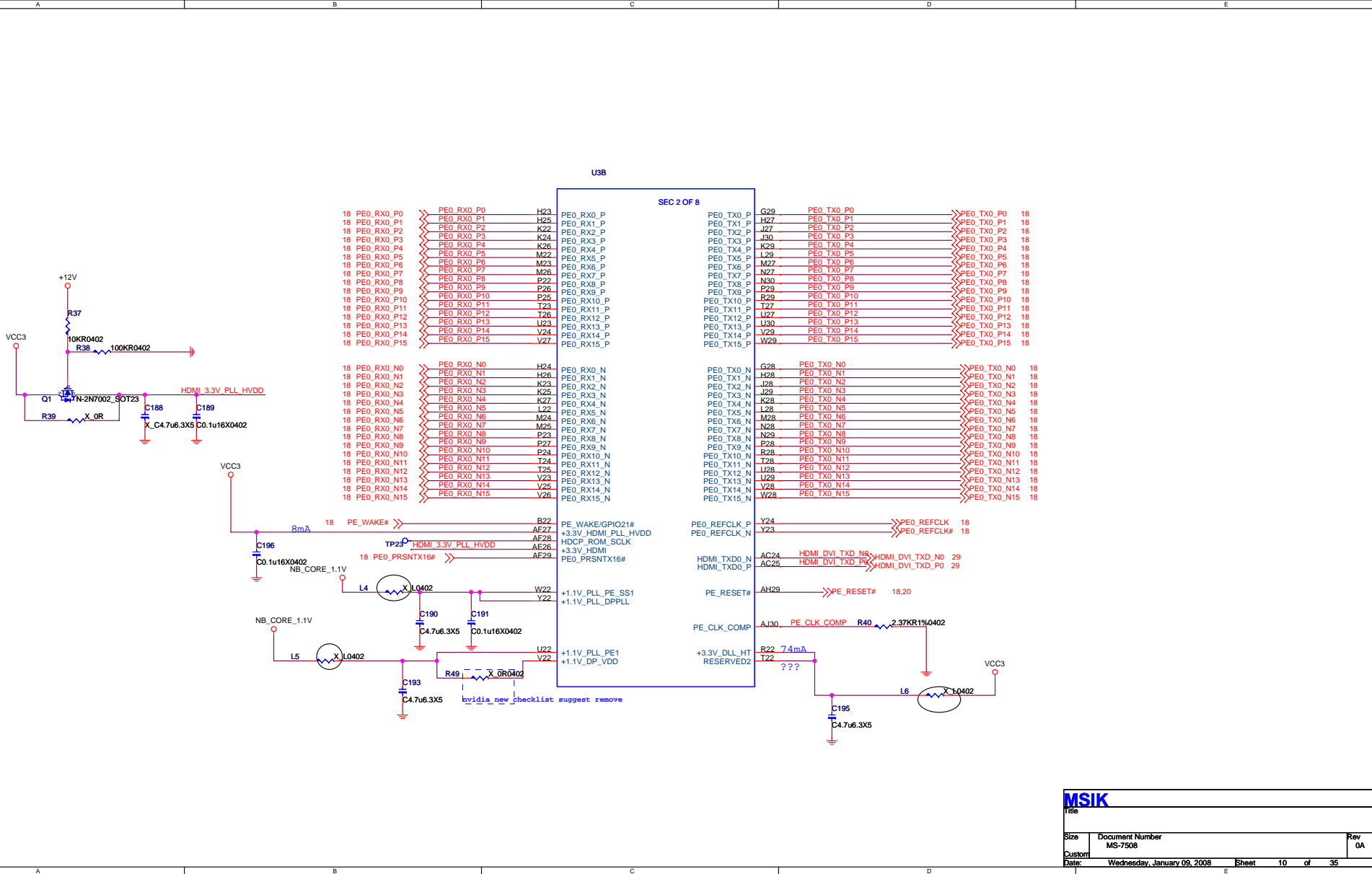
ADDRESS A6





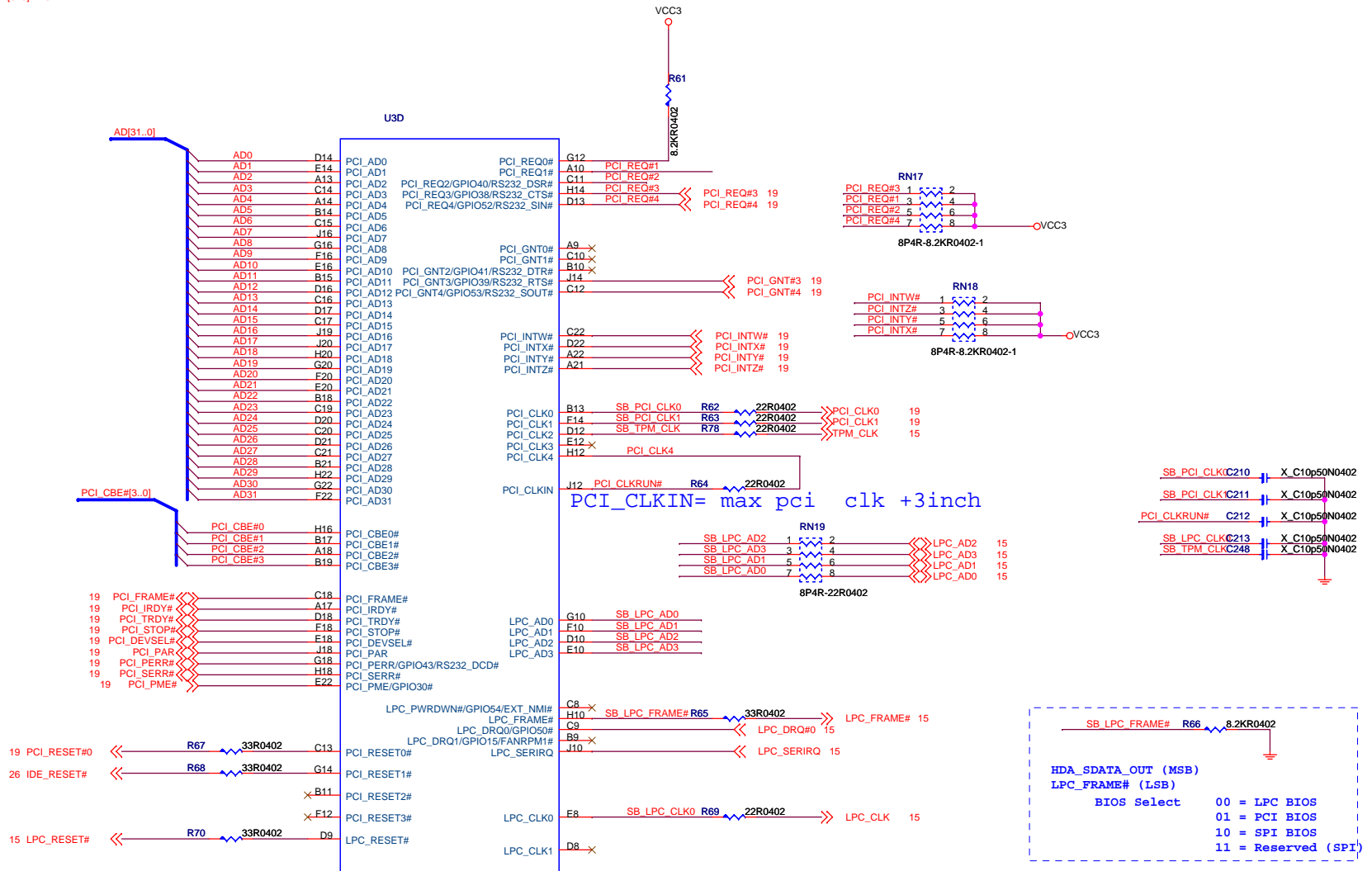




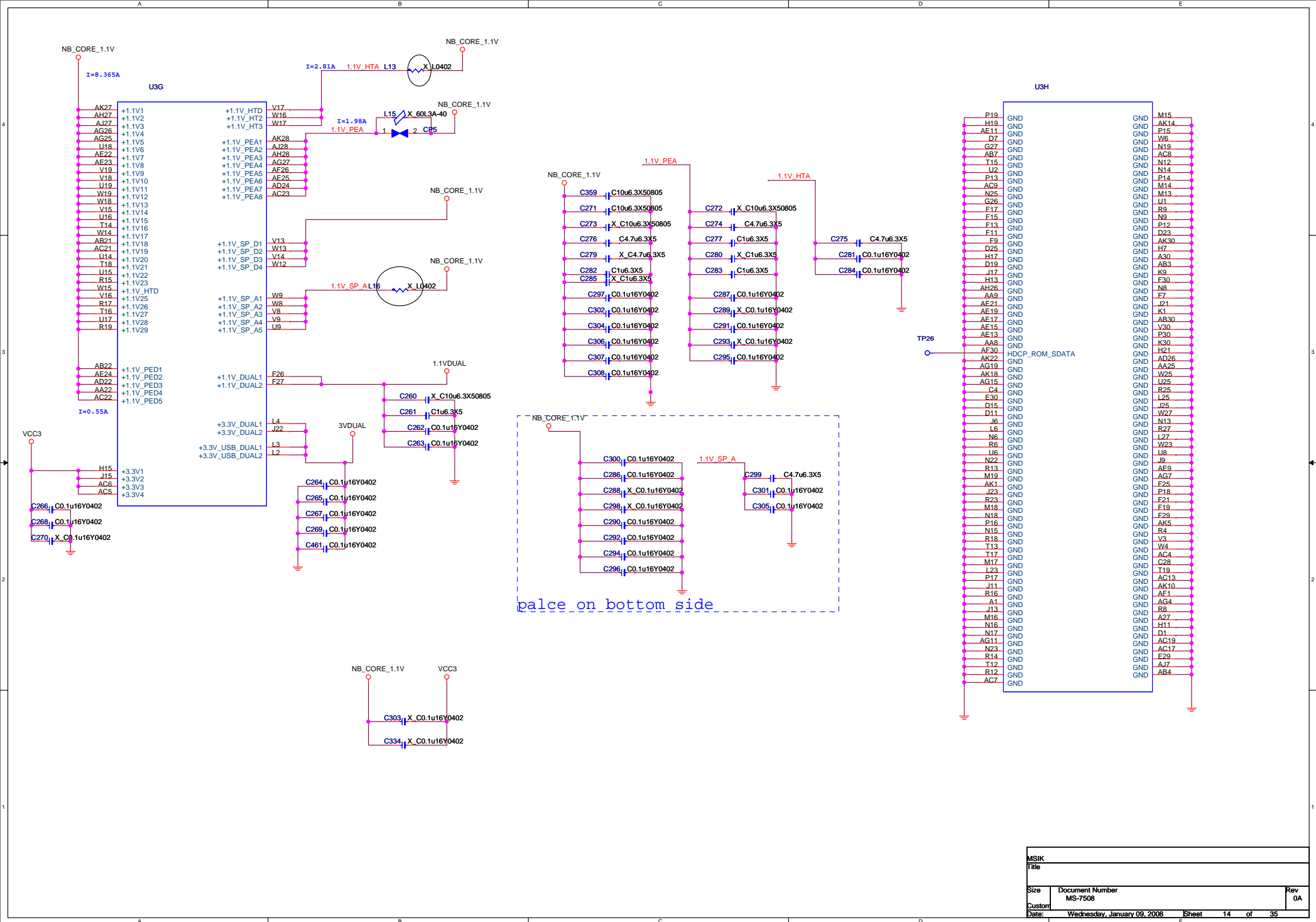


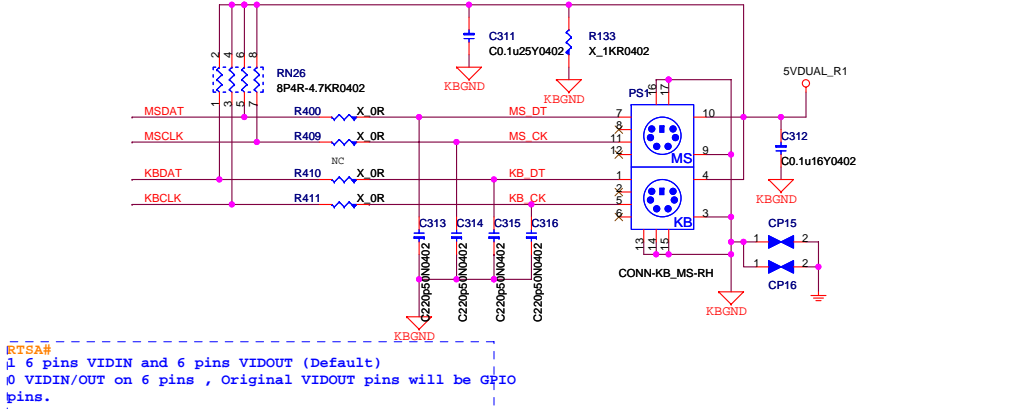
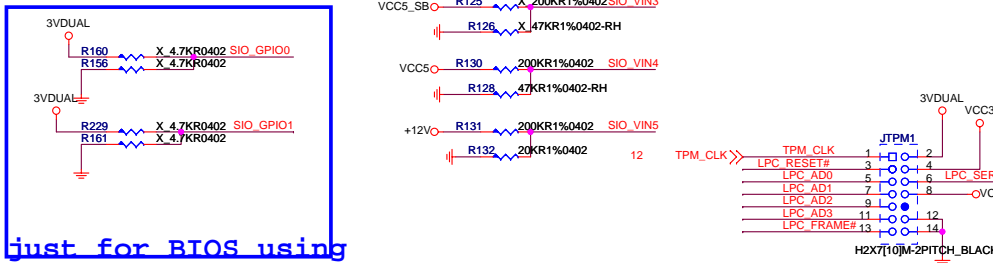


AD[31..0] <<> AD[31..0] 19  
PCI\_CBE#[3..0] <<> PCI\_CBE#[3..0] 19









R142 X 10KR0402 SIO\_FWH\_TRAP  
 R143 1KR0402  
 R144 X 1KR0402 SIO\_HPWM\_DC  
 R146 1KR0402 SIO\_SPI\_TRAP  
 VCC3 R147 X 10KR0402 DTRA#  
 R148 1KR0402  
 R150 1KR0402 RTSA#  
 R151 X 1KR0402 SOUTA

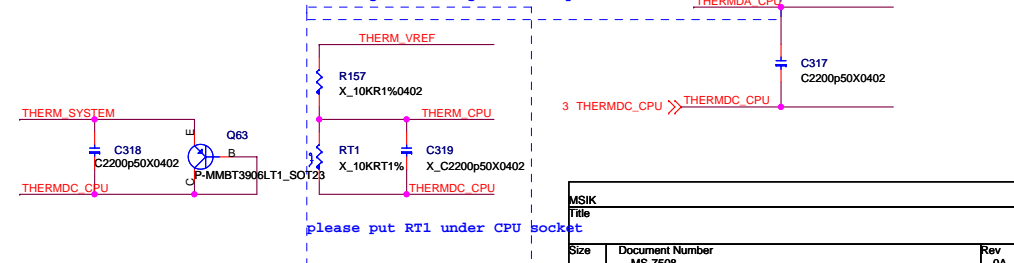
SIO\_FWH\_TRAP  
 1 SPI as a backup BIOS (Default) 1 FWH\_TRAP  
 0 SPI as a primary BIOS

SIO\_HPWM\_DC  
 1 Fan control mode: PWM mode. ( Default) HPWM\_DC  
 0 Fan control mode: Linear mode.

SIO\_SPI\_TRAP  
 1 SPI function disable (Default)  
 0 SPI function enable

DTRA#  
 1 Power on Fan speed default duty is 60%(PWM)(Default)  
 0 Power on Fan speed default duty is 100%(PWM)

SOUTA  
 1 Configuration Register I/O port is 4E/4F. (Default)  
 0 Configuration Register I/O port is 2E/2F. THERMAL\_CTL

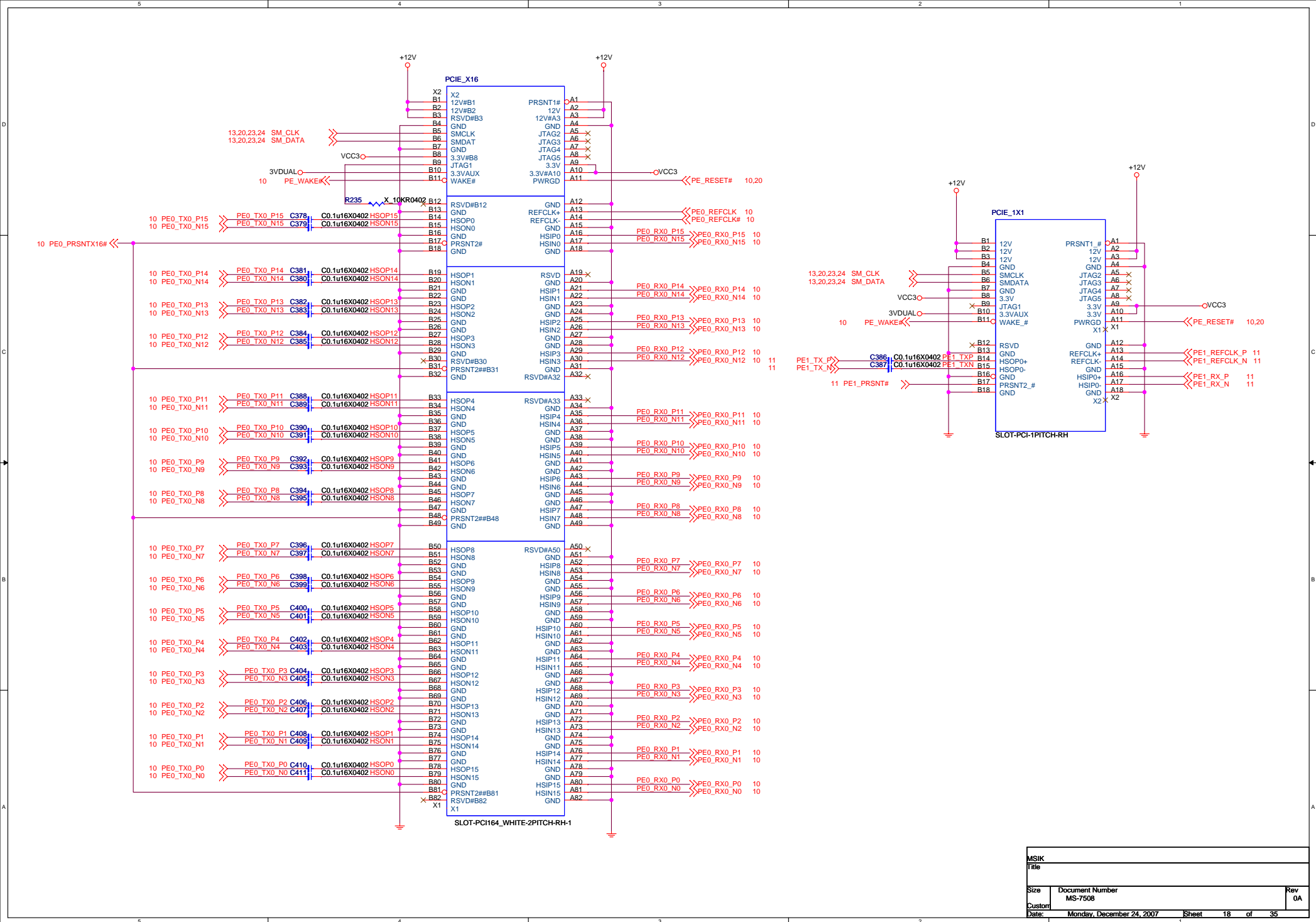


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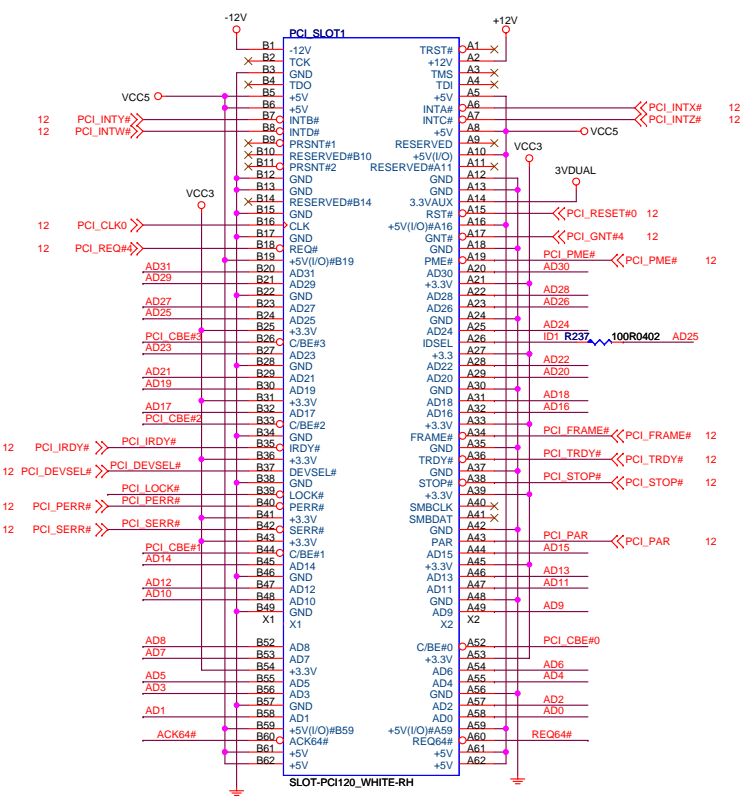




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12 AD[31..0] >> AD[31..0]  
12 PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

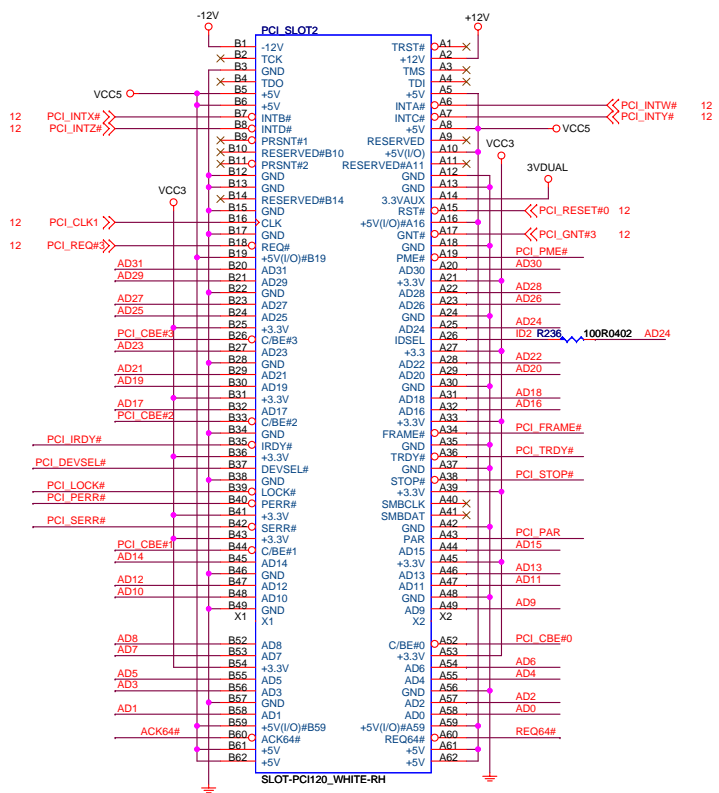
### PCI SLOT 1 (PCI VER: 2.3 COMPLY)



ISSEL = AD25  
MASTER = PCI\_REQ#4  
PCI\_GNT#4

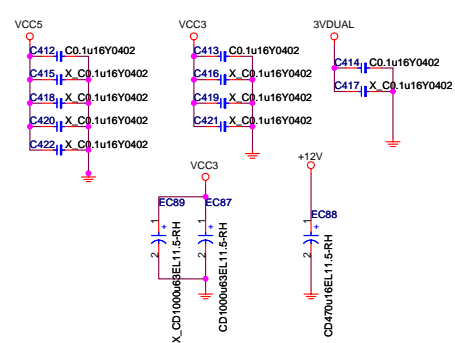
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12 PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

### PCI SLOT 2 (PCI VER: 2.3 COMPLY)

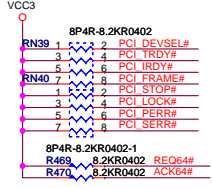


ISSEL = AD24  
MASTER = PCI\_REQ#3  
PCI\_GNT#3

### PCI SLOT DECOUPLING CAPACITORS

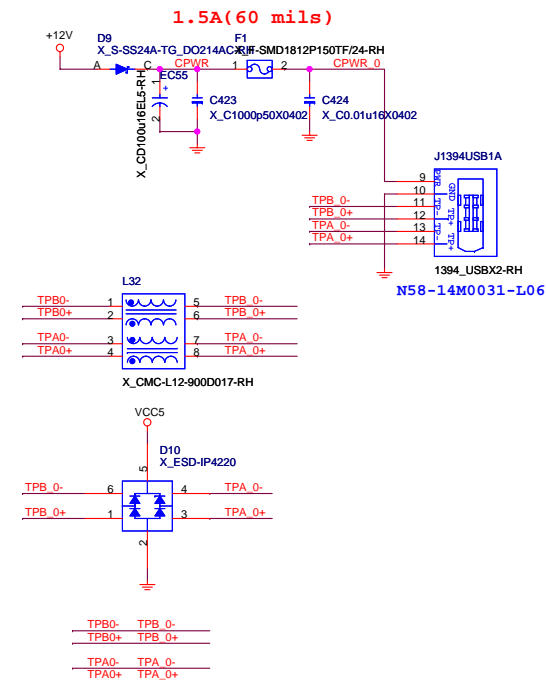


### PCI PULL-UP / DOWN RESISTORS

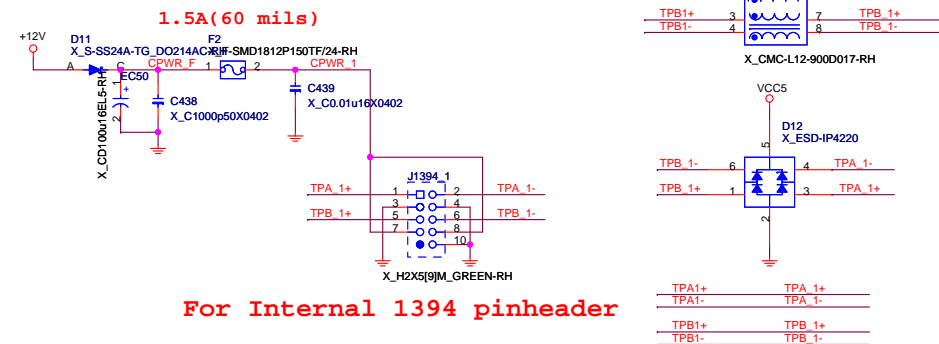


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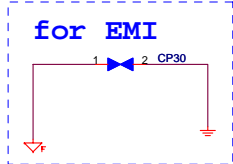
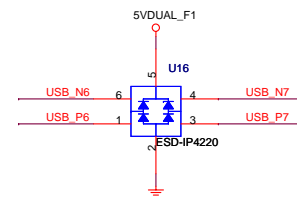
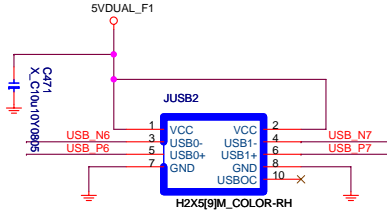
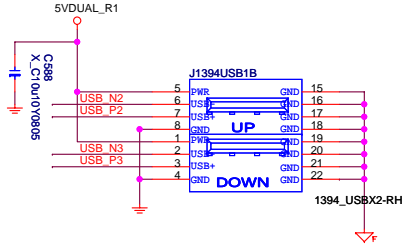
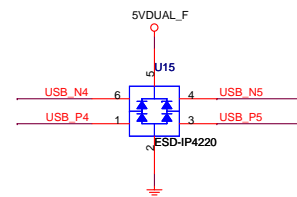
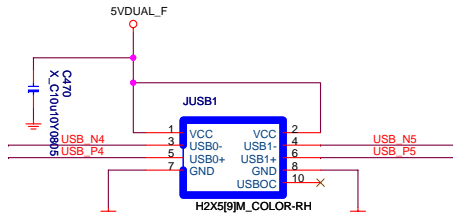
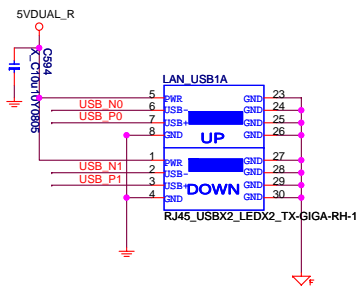
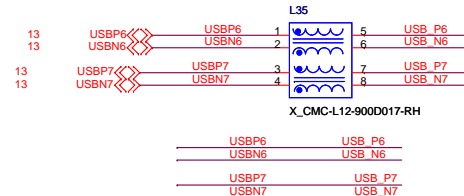
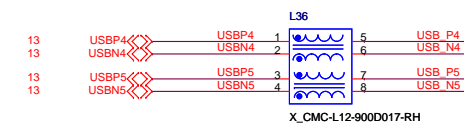
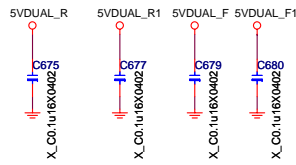
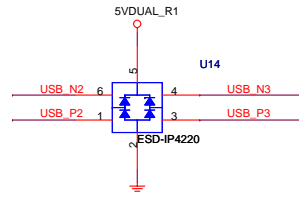
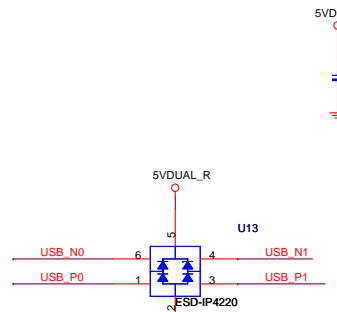
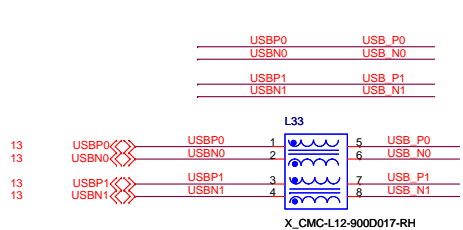
**Rear 1394 port**



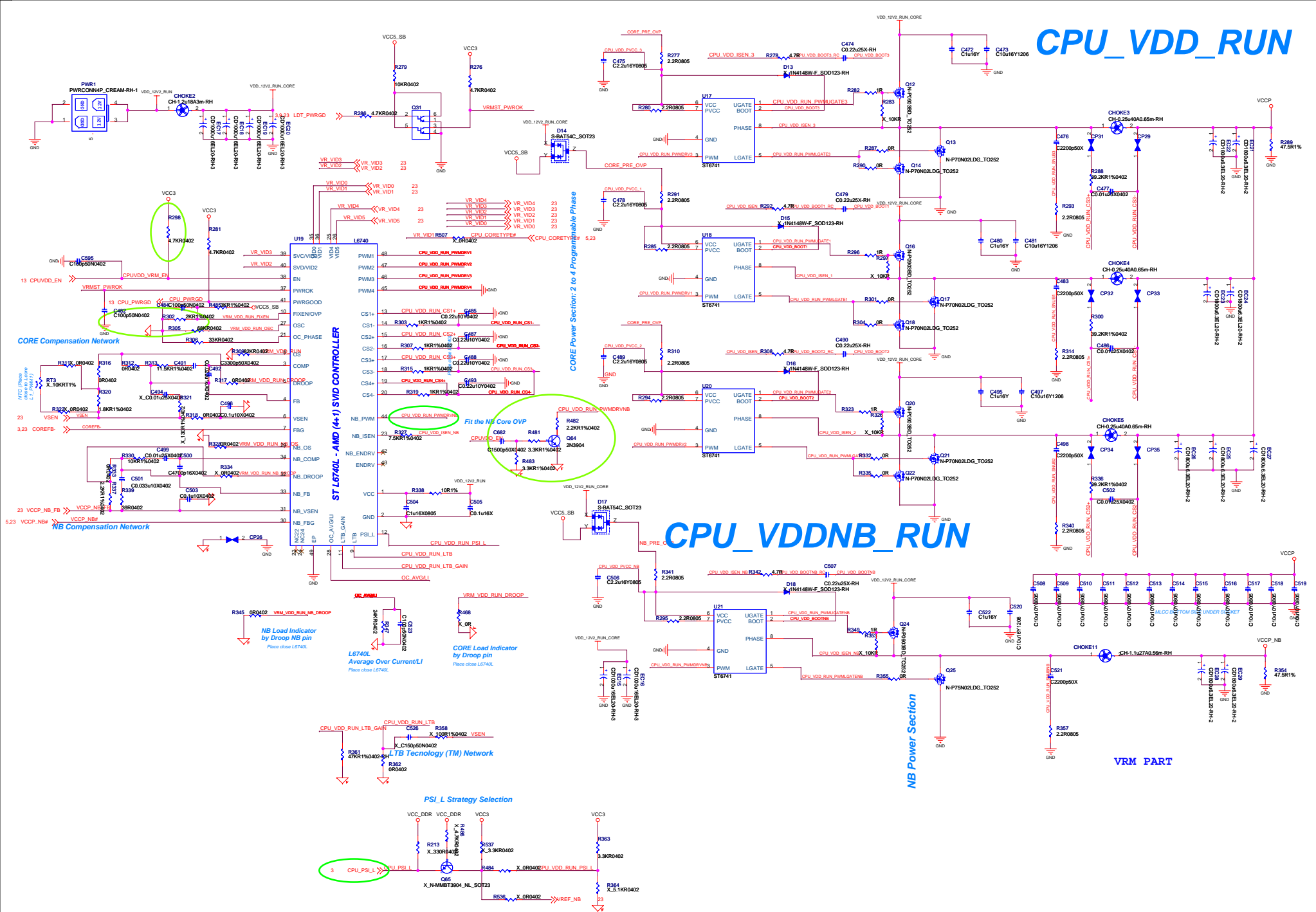
**.5A(60 mils)**



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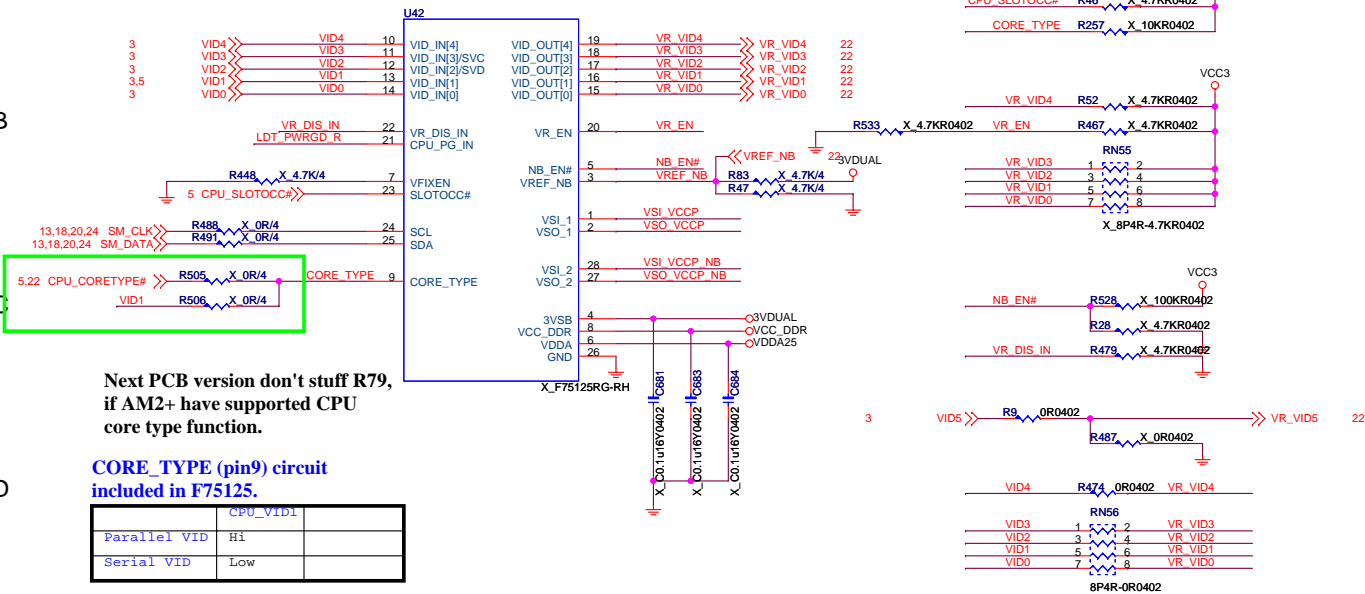


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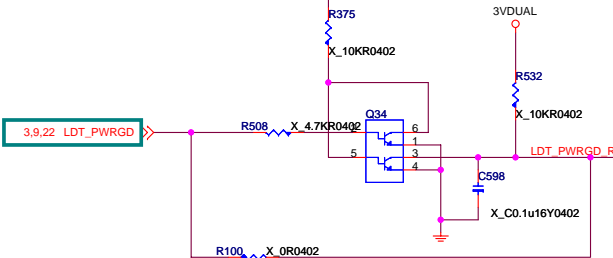
## FINTEK75125 : VCCP & VCCP\_NB OV



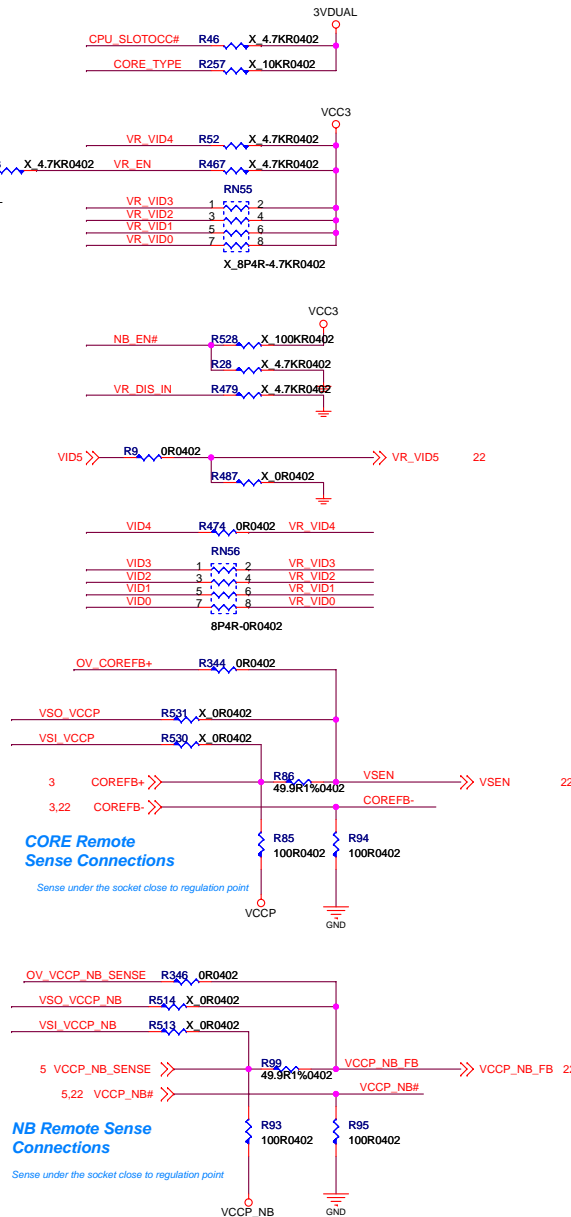
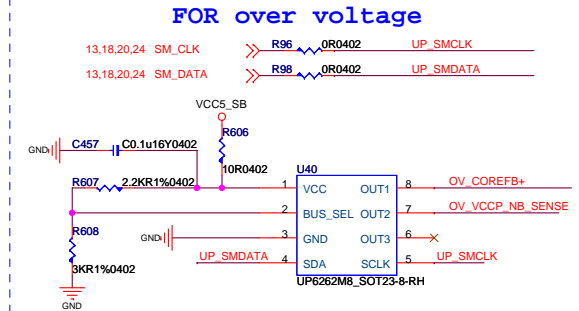
**Next PCB version don't stuff R79, if AM2+ have supported CPU core type function.**

**CORE\_TYPE (pin9) circuit  
included in F75125.**

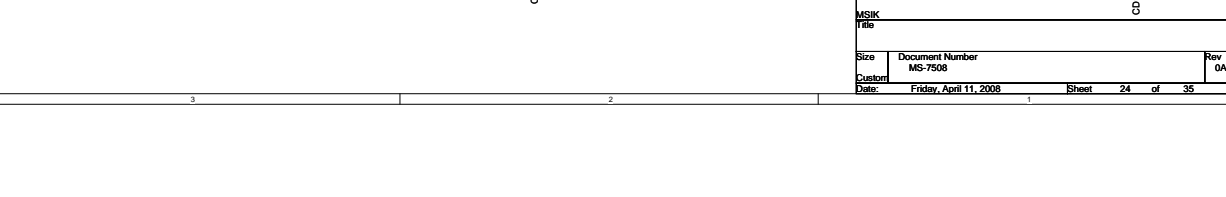
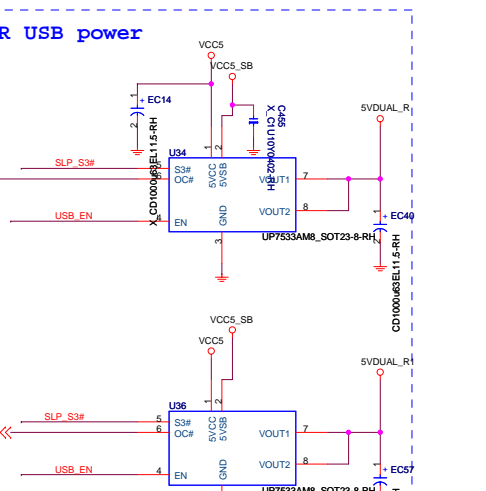
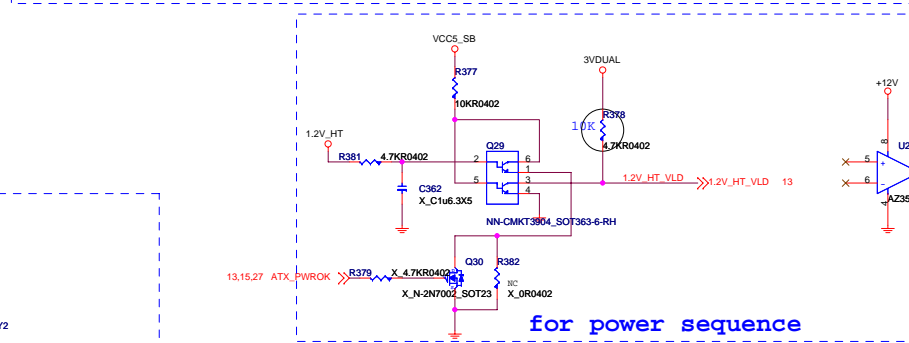
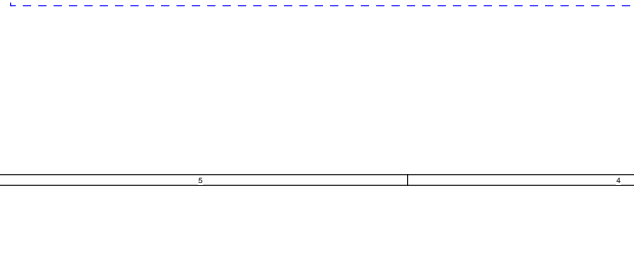
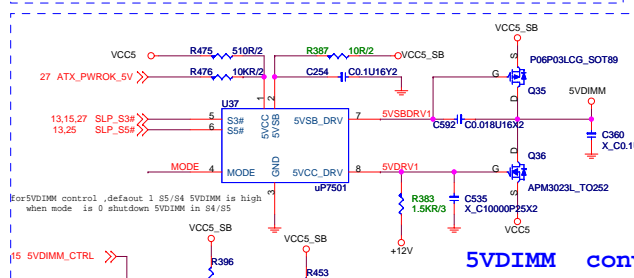
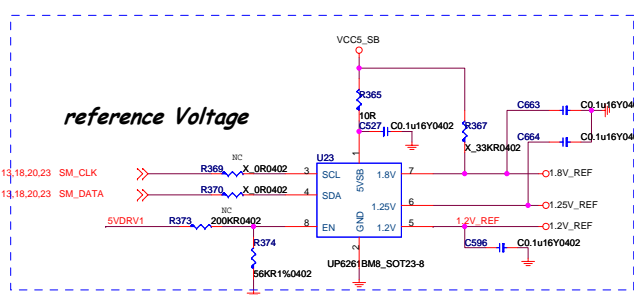
	CPU_VID1	
Parallel VID	Hi	
Serial VID	Low	



FOR over voltage



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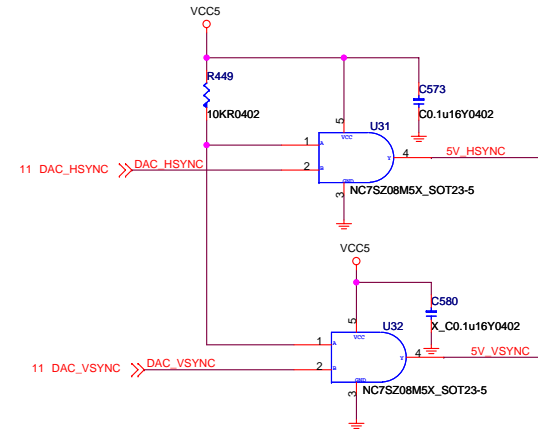
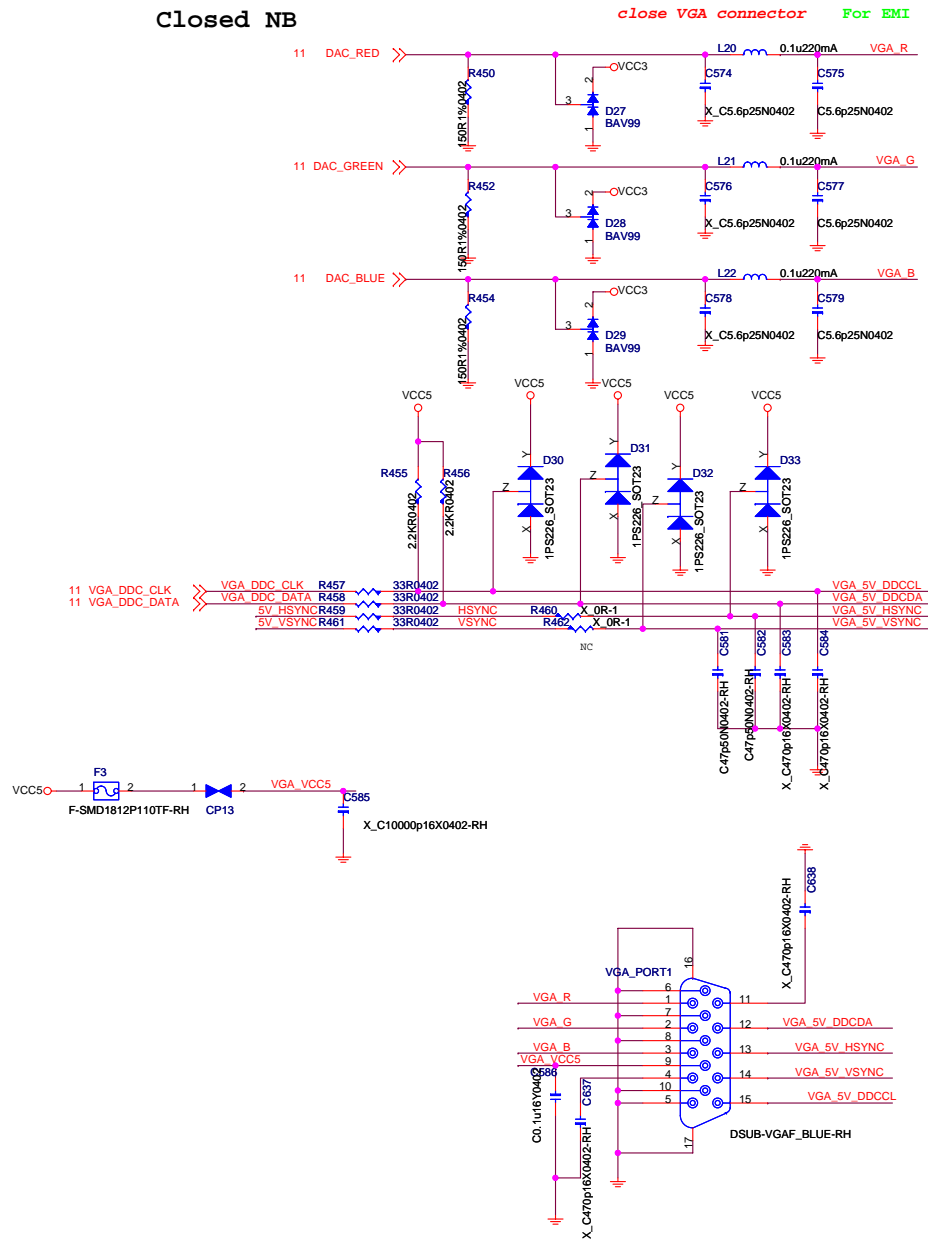






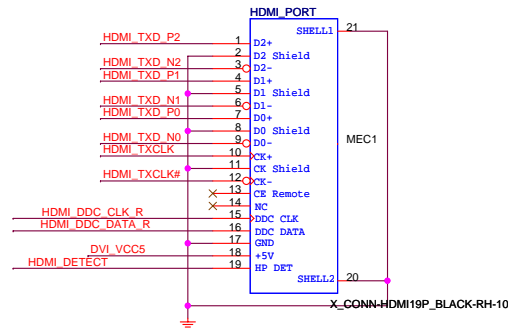
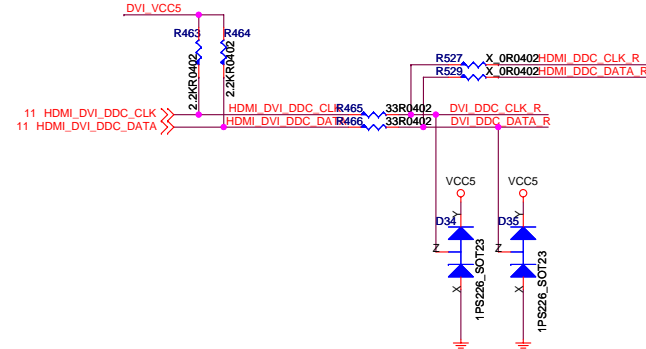
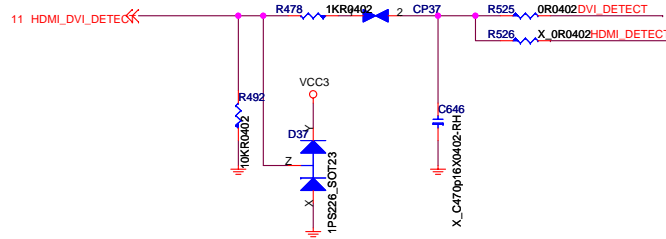
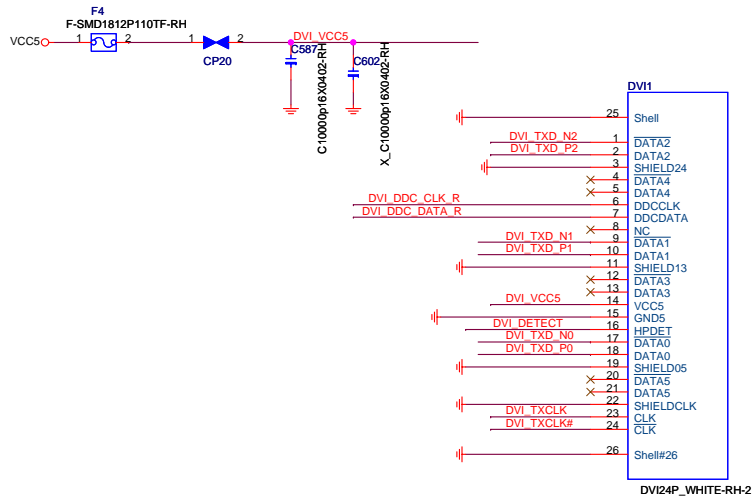
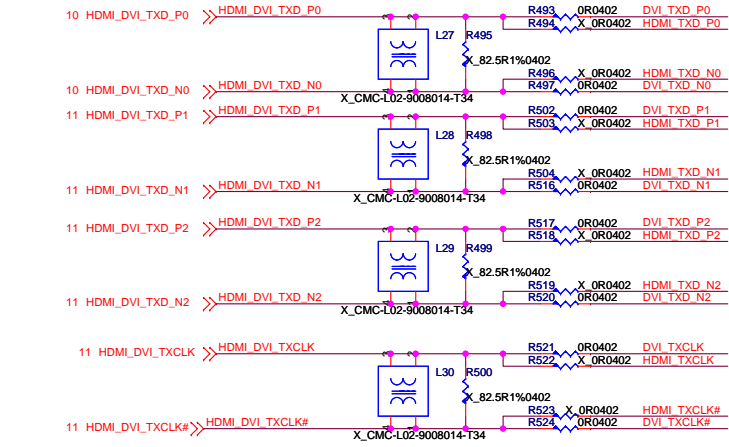
## VGA CONNECTOR

Closed NB



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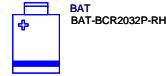
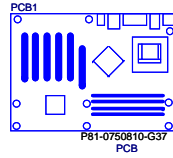
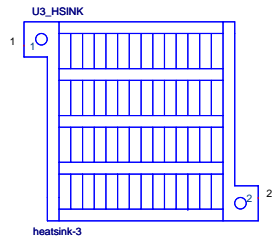
for EMI place near DVI connector



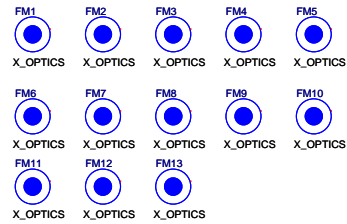
R501 90.9R1%0402  
for HDMI EMI used

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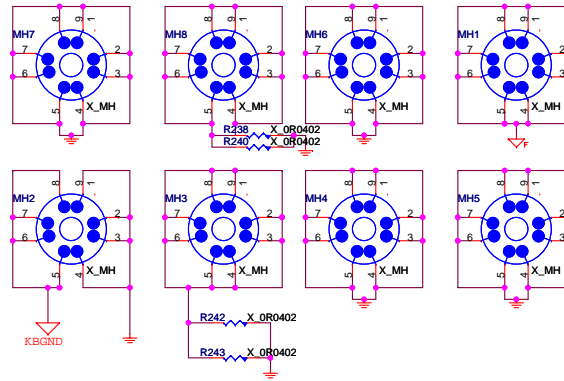




### Optics Orientation Holes



### Mounting Holes



### Simulation



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7508	MCP78+RTL8211BL+ALC888+2PCI+1PCIEX16+1PCIEX1+2PS2+8USB+2COM+HDMI/DVI/VGA+1Audio+RJ45	Cfg-7508VOA	

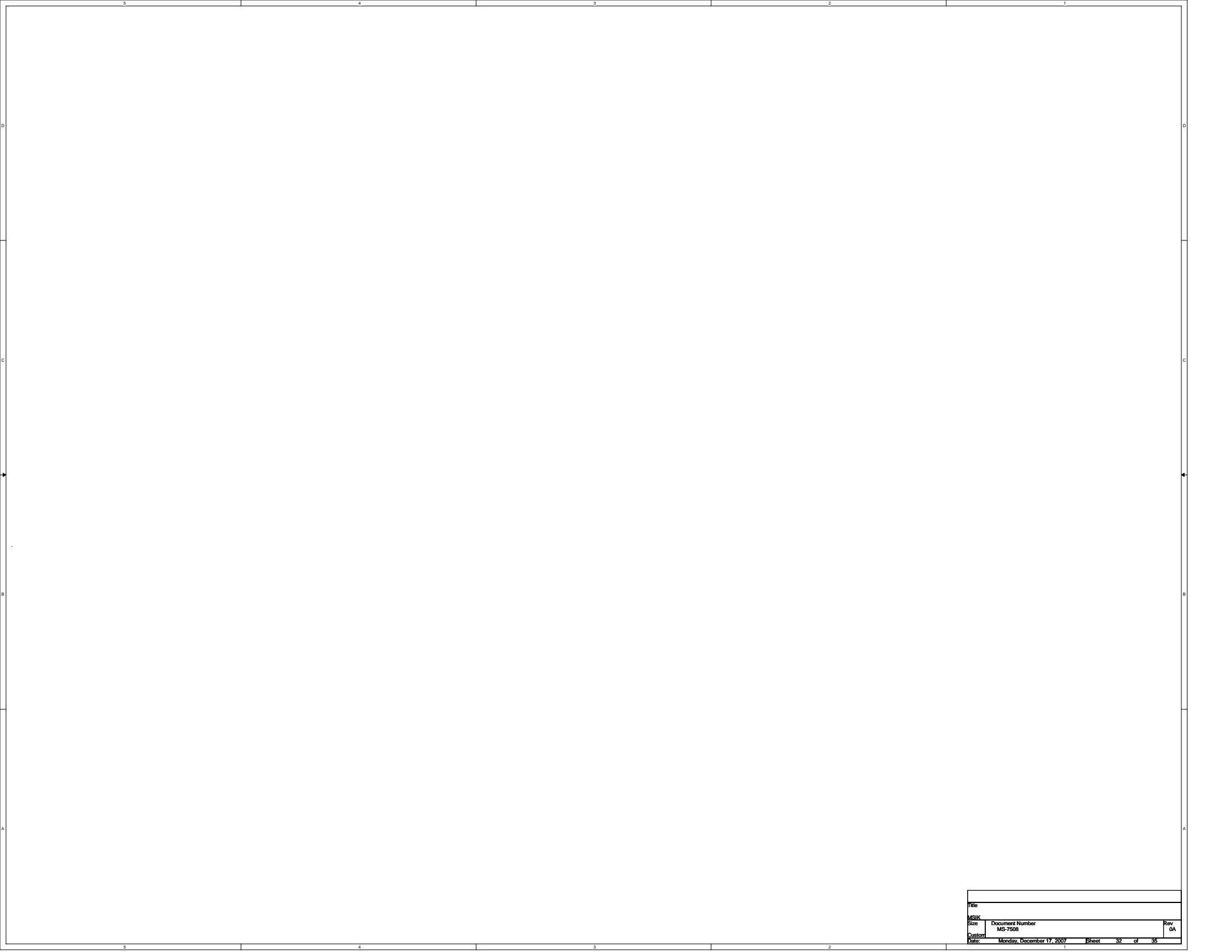
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MS7508V0A

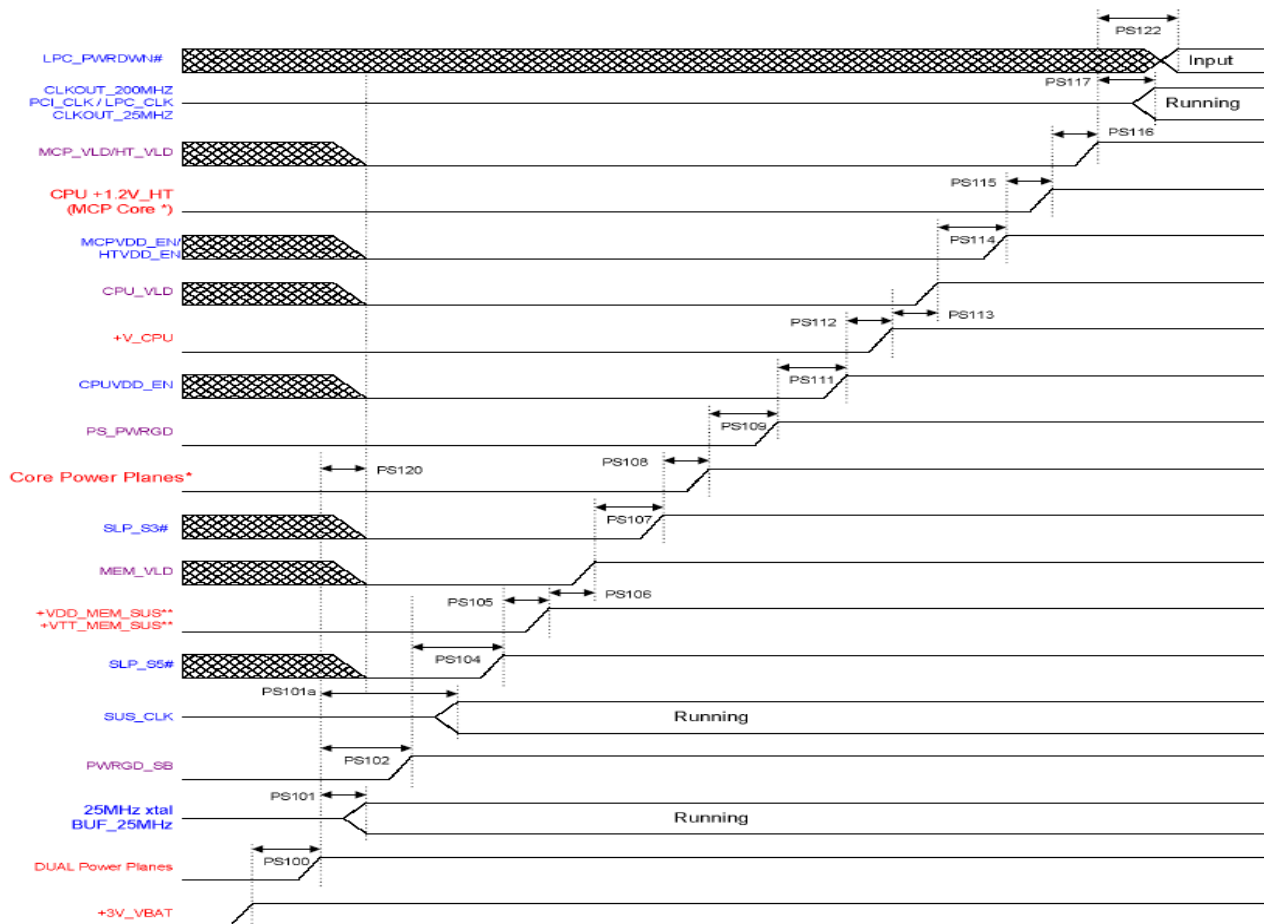
- 1 page 23 add 1.2vref 1.8 vref 1.25vref capacitor
- 2 add EMI solution
- 3 add R60 C203 for VGA function and change serial induce to82nH
- 4 add EC33 EC40 EC56 EC57 capacitor for SI test fail issue
- 5 remove c250 c251 for sequence issue
- 6 change R309 to 82K as power suggestion
- 7 change VRM\_EN circuit
- 8 please 0.1uf near the chipset VBAT power pin
- 9 add EMI parallel port capacitor
- 10 co\_lay 75125

change the C193,C195 to 0603  
change the R228 to 1.5K  
change the R65 to 33 ohm  
Add C462,C600  
change PWRGD\_SBY

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**Power Planes are in Red      MCP output signals are in Blue      Motherboard-generated signals to MCP are in Purple**

**\* Core Power Planes include:**  
 All power rails without \_DUAL or \_SUS in the name except:  
 - CPU Core Power  
 - CPU +1.2V\_HT  
 - and optionally, the MCP Core voltage rail

**\*\* Memory Power Planes vary with the memory standard.**  
 - DDR = 2.5, 1.25V  
 - DDR2 = 1.8, 0.9V  
 - DDR3 = 1.5, 0.75V

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